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| APPLICATION NO.                     | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-------------------------------------|-------------|----------------------|---------------------|------------------|
| 10/709,776                          | 05/27/2004  | William G. America   | FIS920040083US1     | 3775             |
| 23550                               | 7590        | 11/30/2006           | EXAMINER            |                  |
| HOFFMAN WARNICK & D'ALESSANDRO, LLC |             |                      | IM, JUNGHWA M       |                  |
| 75 STATE STREET                     |             |                      | ART UNIT            |                  |
| 14TH FLOOR                          |             |                      | PAPER NUMBER        |                  |
| ALBANY, NY 12207                    |             |                      | 2811                |                  |

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/709,776

Applicant(s)

AMERICA, WILLIAM G.

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 21-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 21-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 5, 2006 has been entered.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al (US Pat. 6,255,233), hereinafter Smith.

Regarding claim 1, Fig. 3 of Smith shows a semiconductor device comprising:

a substrate [50;wafer substrate] including silicon;

a dielectric [150,160, 180, 190, 200] atop the substrate, the dielectric layer including a first dielectric sub-layer [200; SiOF] , a second dielectric sub-layer [180; SiN] and a first non-discrete transitional dielectric sub-layer [190; graded silicon oxynitride; col. 3, lines 51-57]

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residing between the first and second dielectric sub-layer layer, wherein the first dielectric sub-layer has an etch resistance different than the second dielectric sub-layer, and

an opening [185] extending no deeper than the sub-layer nearest the substrate.

Regarding claim 2, Fig. 3 of Smith shows that an etch resistance of the first dielectric sub-layer [SiOF] is greater than an etch resistance of the second dielectric sub-layer [SiN].

Regarding claim 3, Fig. 3 of Smith shows that the first dielectric sub-layer [SiOF; fluorinated silicon oxide] has a greater content of fluorine than the second dielectric sub-layer [SiN].

Regarding claim 6, Fig. 3 of Smith shows that the dielectric layer includes a third dielectric sub-layer [150; SiN] residing between the substrate and the first dielectric sub-layer and a second non-discrete transitional dielectric sub-layer [160; graded silicon oxynitride; col. 3, lines 51-57] residing between the third dielectric sub-layer and the first dielectric sub-layer.

Regarding claim 7, Fig. 3 of Smith shows that the second dielectric sub-layer [180; SiN] and the third dielectric sub-layer [150; SiN] have substantially the same etch resistance.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-5 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Todd (US Pat. 6,733,830).

Regarding claims 4 and 5, Fig. 3 of Smith shows most aspects of the instant invention except “the first dielectric sub-layer includes at least one component not included in the second dielectric sub-layer, the at least one component being selected from a group consisting of fluoroalkylsilanes, fluoralkylsiloxanes, perfluoroalkylsilanes, perfluoroalkylsiloxanes, alkylsilanes, and alkylsiloxanes while the at least one component is selected from a group consisting of methylsilane, dimethylsilane, trimethylsilane, trifluoromethylsilane, 1,2-disilano-tetrafluoroethylene, 1,3-bis(silano-difluoromethylene)disiloxane, 2,2-disilano-hexafluorosilane, bis(trifluoromethyl-disiloxanyl)difluoromethane, octamethylcyclotetrasiloxane, and tetramethylcyclotetrasiloxane.” Todd discloses the first dielectric sub-layer includes at least one component not included in the second sub-layer, that is, the first dielectric sub-layer being fluorinated through the at least one component being selected from a group consisting of fluoralkylsiloxanes and alkylsilanes (col. 7, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings Todd of into the device of Smith in order to have the first sub-layer including at least one component not included in the second sub-layer, the at least one component being selected from a group consisting of fluoralkylsiloxanes and alkylsilanes to reduce the etch rate.

Regarding claim 21, Fig. 3 of Smith shows a semiconductor device comprising:  
a substrate [50;wafer substrate] including silicon;  
a dielectric [150,160, 180, 190, 200] atop the substrate, the dielectric layer including a first dielectric sub-layer [200; SiOF] , a second dielectric sub-layer [180; SiN] and a first non-discrete transitional dielectric sub-layer [190; graded silicon oxynitride; col. 3, lines 51-57]

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residing between the first and second dielectric sub-layer layer, wherein the first dielectric sub-layer has an etch resistance different than the second dielectric sub-layer, and

an opening [185] extending no deeper than the sub-layer nearest the substrate.

Fig. 3 of Smith shows most aspects of the instant invention except the first sub-layer includes at least one component not included in the second sub-layer, the at least one component being selected from a group consisting of fluoroalkylsilanes, fluoralkylsiloxanes, perfluoroalkylsilanes, perfluoroalkylsiloxanes. Todd discloses the first dielectric sub-layer includes at least one component not included in the second sub-layer, that is, the first dielectric sub-layer being fluorinated through the at least one component being selected from a group consisting of fluoralkylsiloxanes and alkylsilanes (col. 7, lines 48-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings Todd of into the device of Smith in order to have the first sub-layer including at least one component not included in the second sub-layer, the at least one component being selected from a group consisting of fluoralkylsiloxanes and alkylsilanes to reduce the etch rate.

Regarding claim 22, Fig. 3 of Smith shows that an etch resistance of the first dielectric sub-layer [SiOF] is greater than an etch resistance of the second dielectric sub-layer [SiN].

Regarding claim 23, Fig. 3 of Smith shows that the first dielectric sub-layer [SiOF; fluorinated silicon oxide] has a greater content of fluorine than the second dielectric sub-layer [SiN].

Regarding claim 24, Todd discloses the first dielectric sub-layer includes at least one component not included in the second sub-layer, that is, the first dielectric sub-layer being

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fluorinated through the at least one component being selected from a group consisting of methylsilane, dimethylsilane, trimethylsilane, trifluoromethylsilane, 1,2-disilano-tetrafluoroethylene, 1,3-bis(silanodifluoromethylene)disiloxane, 2,2-disilano-hexafluorosilane, bis(trifluoromethylsiloxy)dimethylsilane, octamethylcyclotetrasiloxane, and tetramethylcyclotetrasiloxane (col. 7, lines 48-55).

Regarding claim 25, Fig. 3 of Smith shows that the dielectric layer includes a third dielectric sub-layer [150; SiN] residing between the substrate and the first dielectric sub-layer and a second non-discrete transitional dielectric sub-layer [160; graded silicon oxynitride; col. 3, lines 51-57] residing between the third dielectric sub-layer and the first dielectric sub-layer.

Regarding claim 26, Fig. 3 of Smith shows that the second dielectric sub-layer [180; SiN] and the third dielectric sub-layer [150; SiN] have substantially the same etch resistance.

### ***Response to Arguments***

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

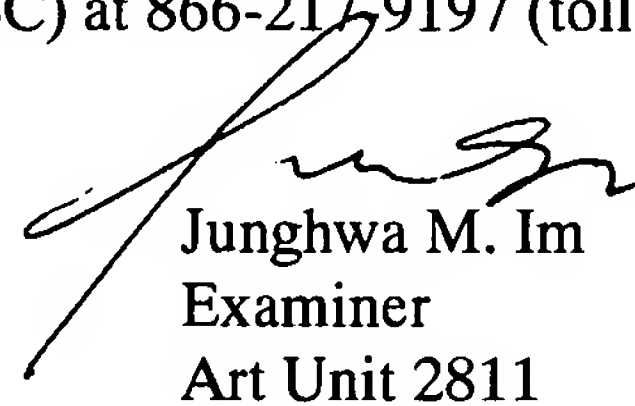
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Junghwa M. Im  
Examiner  
Art Unit 2811

jmi  
11/25/2006